

FIG. 10



FIG. 1a

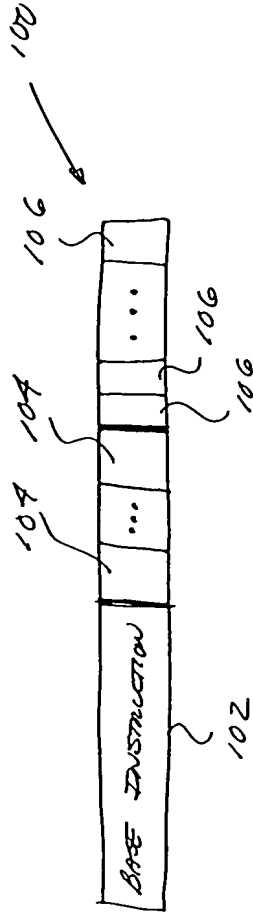


FIG. 1b

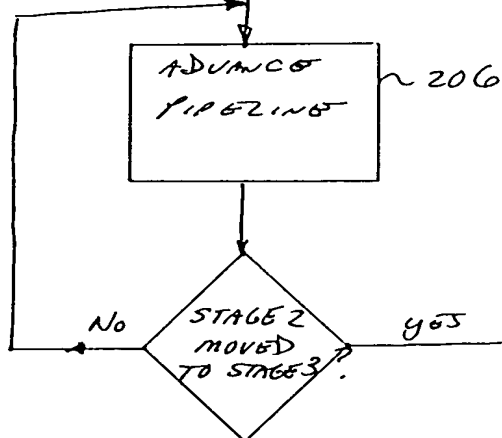


START

DEFINE  
SLEEP  
MODE ~ 202

INSERT  
SLEEP MODE ~ 204  
INSTRUCTION  
IN PIPELINE

ADVANCE  
PIPELINE ~ 206



SET  
ZC FLAG ~ 208

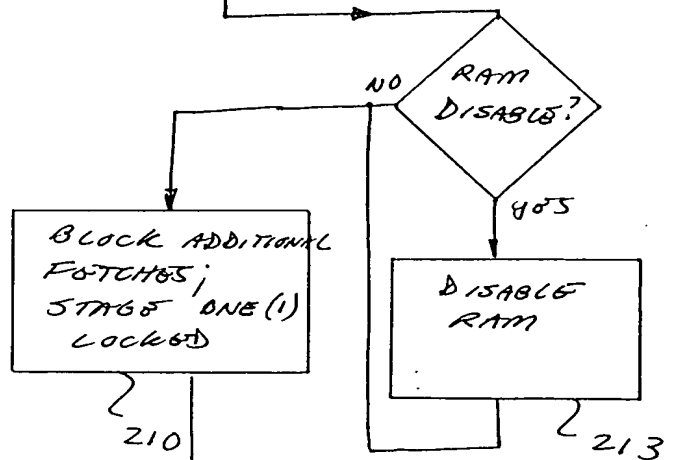
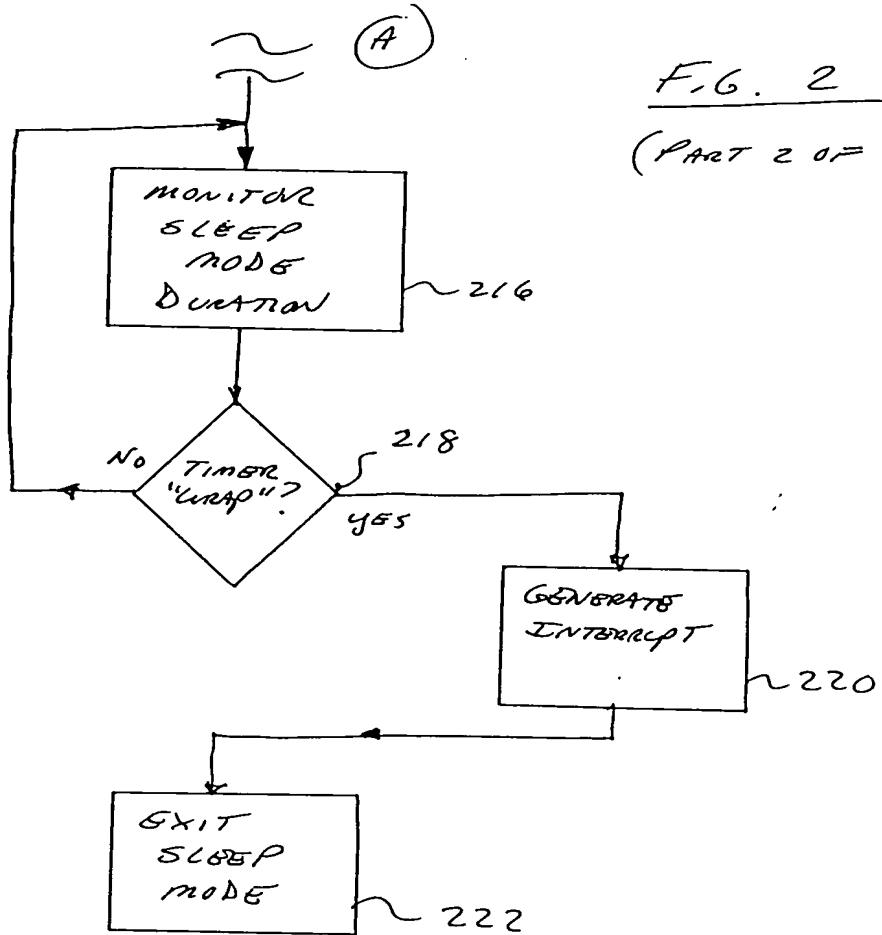


FIG. 2  
(PART 1 OF 2)

FIG. 2  
(PART 2 OF 2)



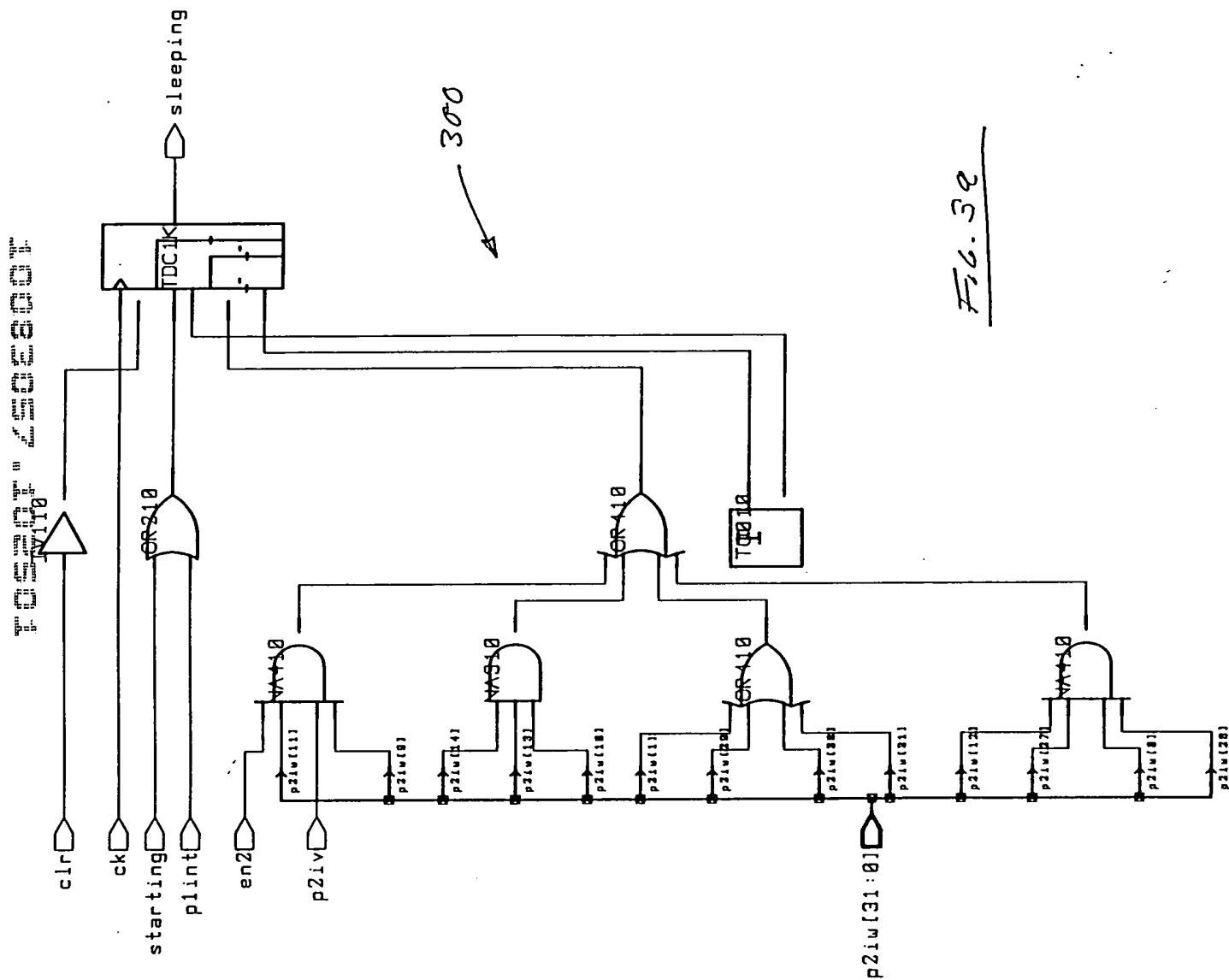


Fig. 5a

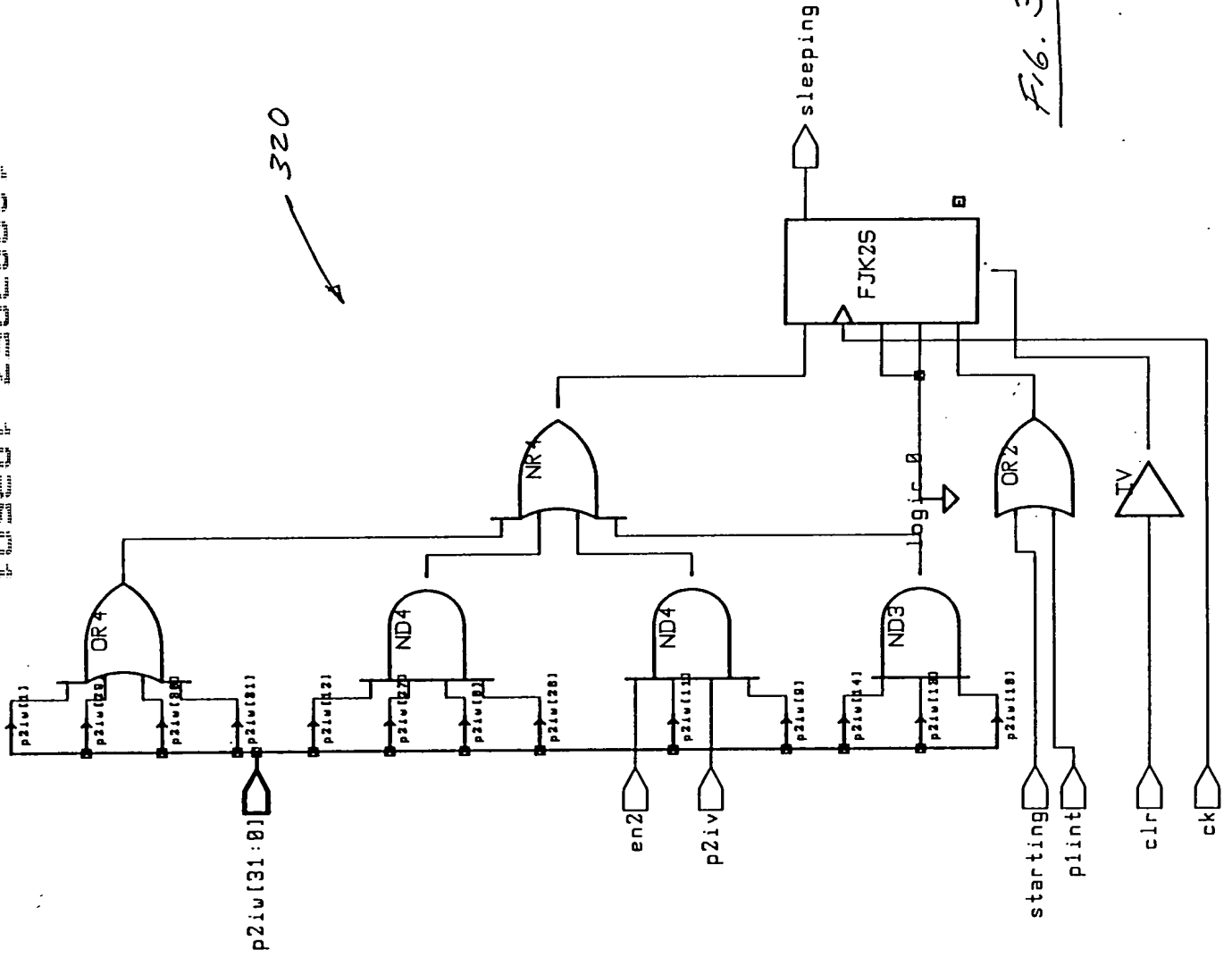


Fig. 3b

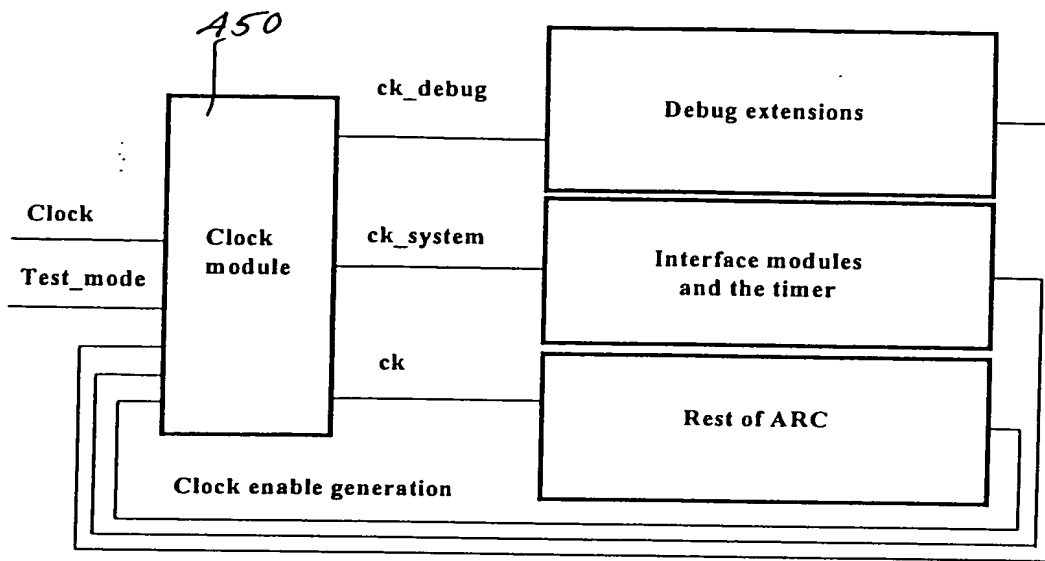


Fig. 4a

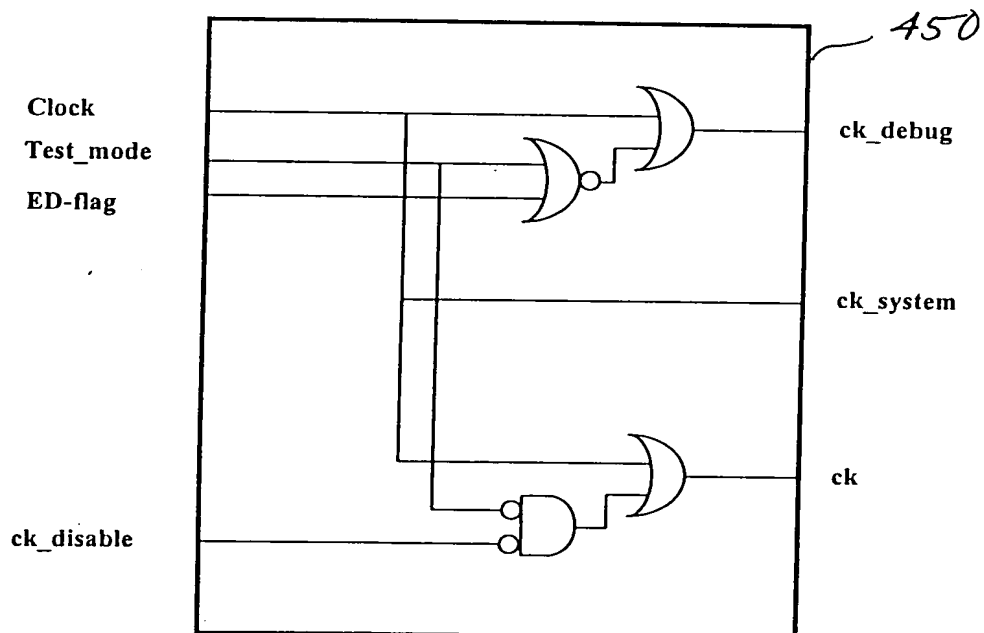


Fig. 4b

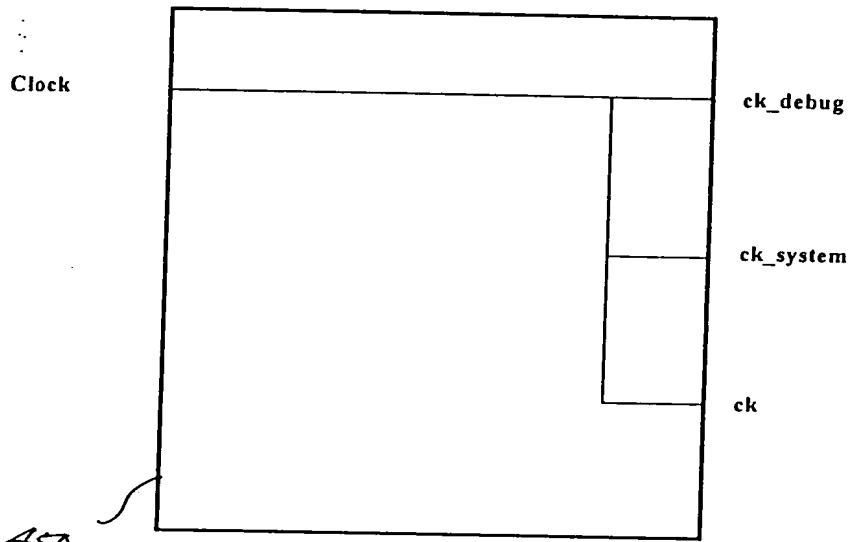
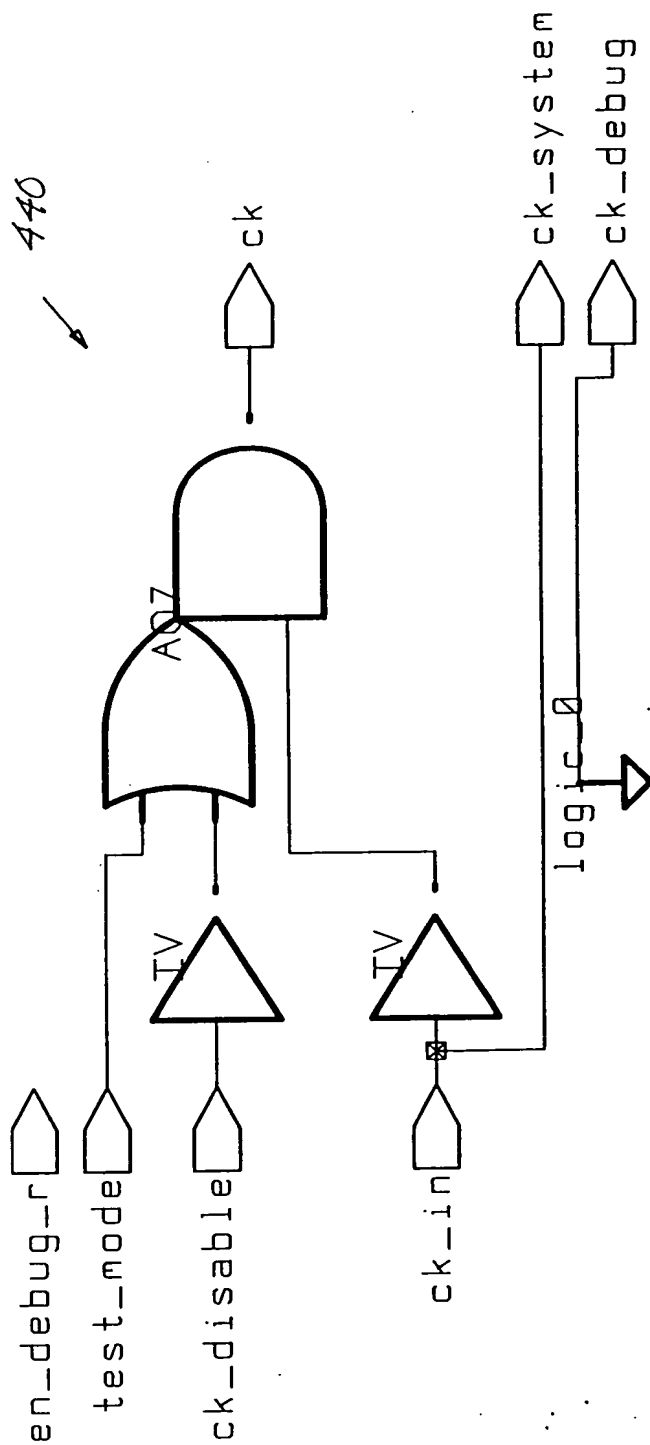


Fig. 4c



Fig. 4d





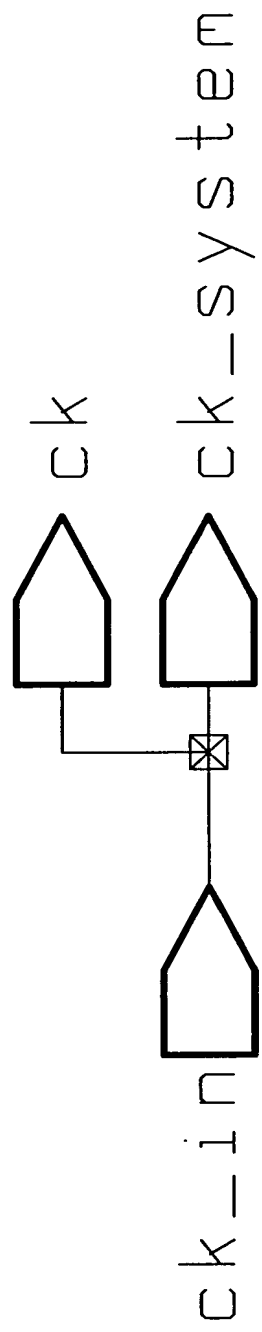
ck\_disable  
en\_debug\_r  
test\_mode

480

Fig. 4f.

logic=0

ck\_debug



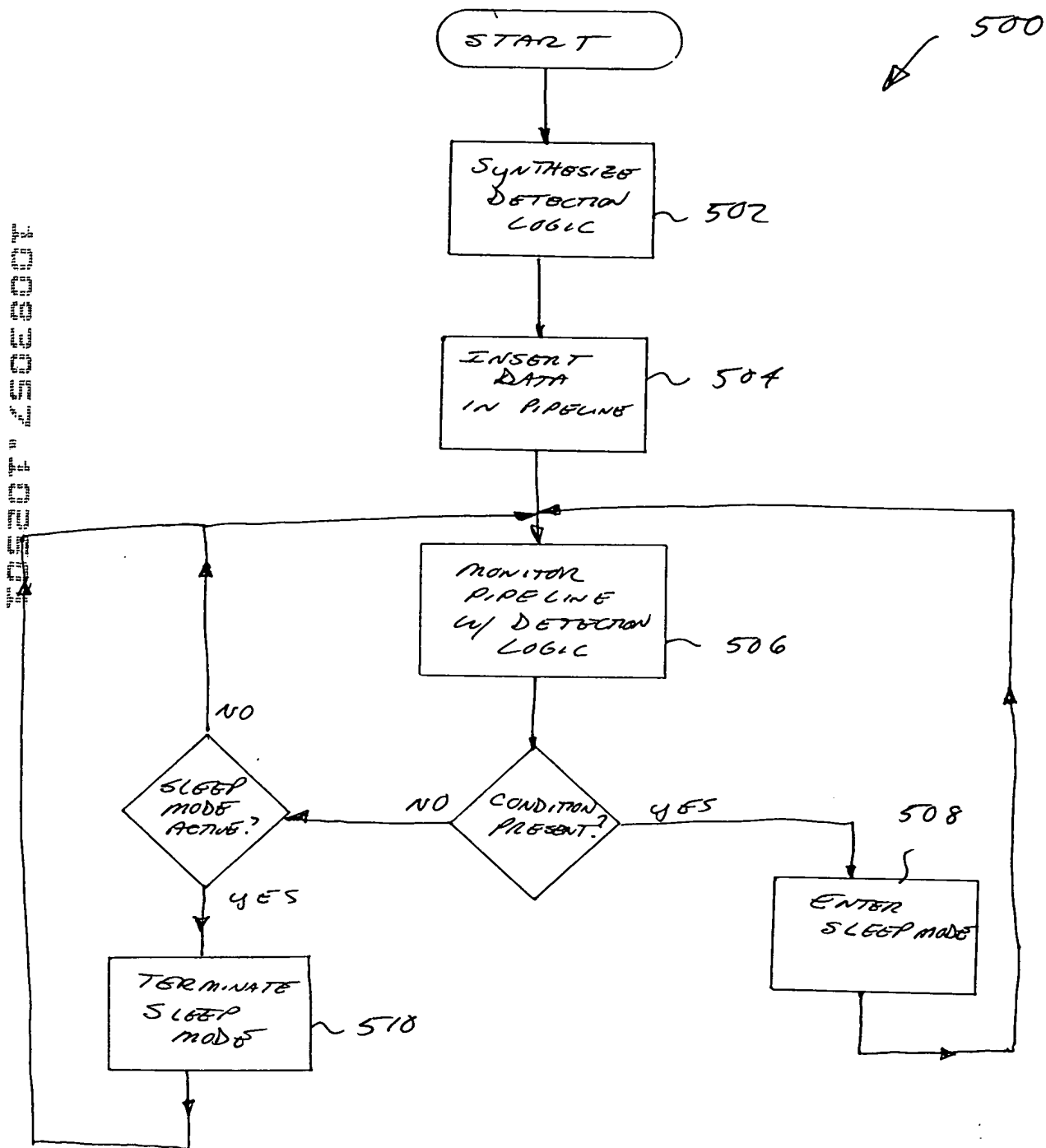


FIG. 5

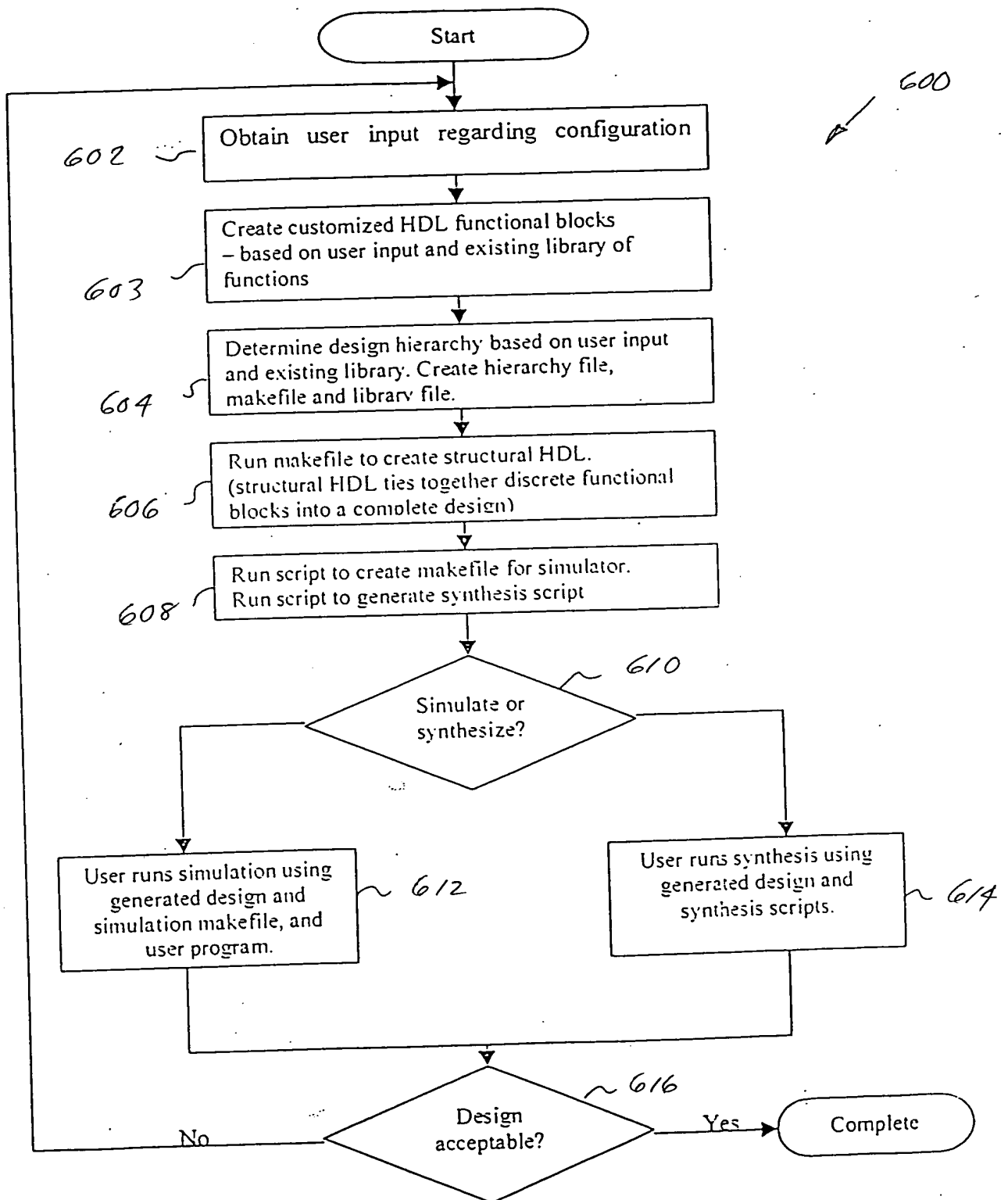


FIG. 6

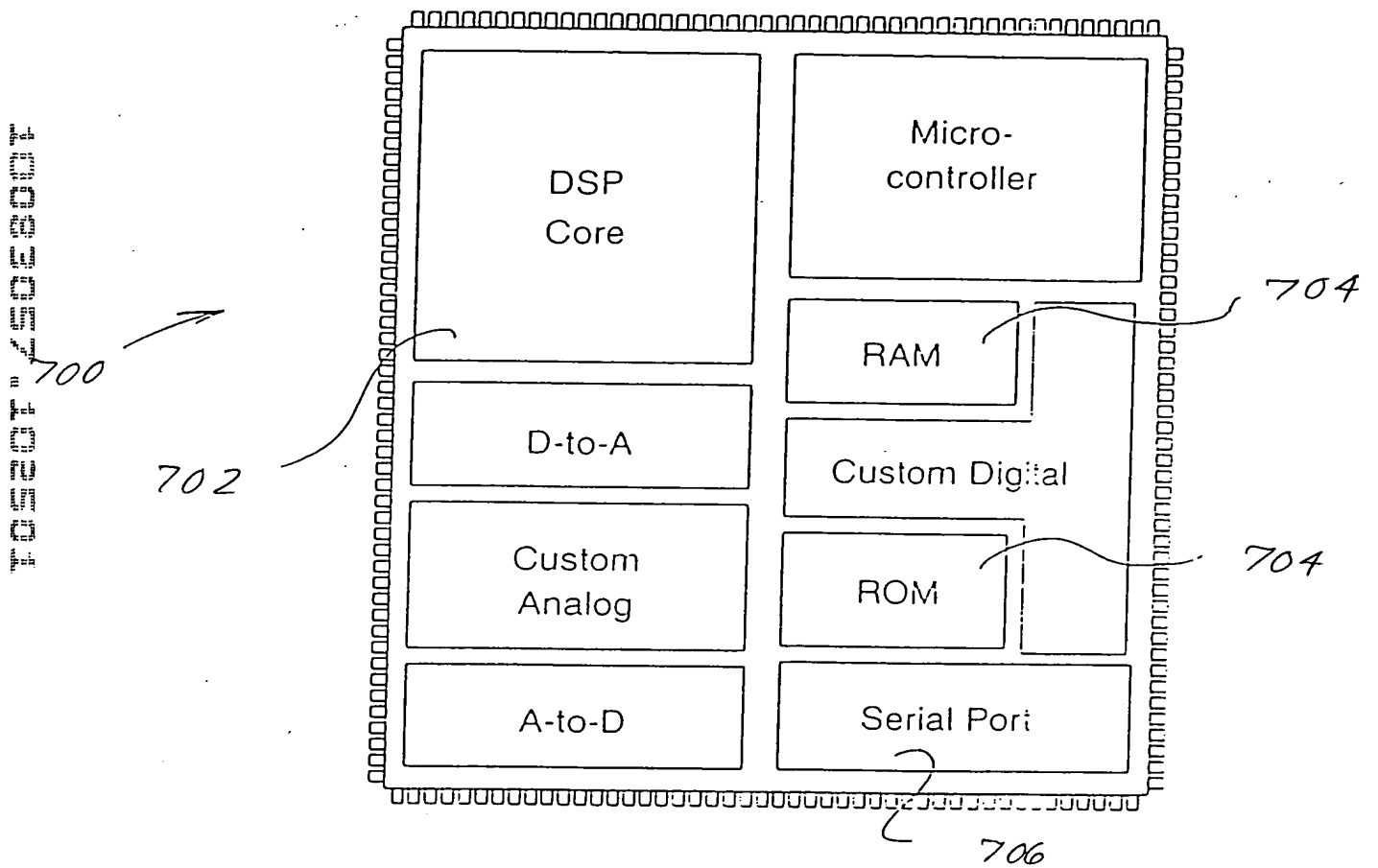


FIG. 7

$$\begin{array}{r} 8 \\ \hline 46 \end{array}$$
